UNIVERSIDADE FEDERAL DE SANTA CATARINA
Centro Tecnológico
Departamento de Informática e Estatística
Programa de Pós-Graduação em Ciência da Computação

COURSE PROGRAM

A critério do professor, não havendo alunos estrangeiros matriculados, a disciplina poderá ser ofertada em língua portuguesa.

1) Identification

Course: INE410133 - Electronic Design Automation (Automação do Projeto Eletrônico)
Workload: 60 horas-aula (4 créditos)
Instructor: José Luís Almada Güntzel
Semester: 2018/2 until the present date.

2) Courses: Master and Doctorate

3) Prerequisites:

Knowledge of programming, data structures and digital design proved through undergraduate and/or graduate courses successfully followed.

4) Overview:

The Electronic Design Automation (EDA) design flow, fundamental algorithms, Electronic System-Level (ESL) design and High-Level Synthesis (HLS), Logic Synthesis (LS), verification and test, Physical Synthesis (PS), implementation issues on selected problems.

5) Course Objectives

General:

Provide a broad view of the electronic design automation of contemporary VLSI circuits.

Specifics Objectives:

- Present the different levels of abstraction of the representation of contemporary digital systems, relating them to the respective stages of synthesis and CMOS manufacturing technology;
- Provide an understanding of the characteristics and requirements of each step of digital circuit synthesis, presenting the usual formulations of each step;
- Present and discuss the most important algorithms and techniques for the various synthesis steps, possibly correlating the respective algorithms to the most appropriate data structures;
- Allow students to go into the details of a technique/algorithm related to one of the synthesis steps by implementing a prototype.

6) Contents:

- Contemporary VLSI design flow and typical Electronic Design Automation (EDA) flow.
- Basic CMOS gates, CMOS fabrication technology and design rules.
- Fundamental algorithms:
    - Computational complexity;
    - Graph algorithms;
    - Heuristic algorithms;
    - Mathematical programming.
- Electronic System-Level (ESL) Design and High-Level Synthesis (HLS):

    - ESL design methodologies;
    - Fundamentals of HLS;
    - Scheduling;
    - Register Biding;
    - Functional unit biding.
- Logic Synthesis (LS):
    - Data structure for Boolean representation;
    - Combinational logic minimization;
    - Technology mapping;
    - Timing analysis and optimization.
- Fault Simulation, Test Synthesis and Verification:
    - Fault models and fault simulation;
    - Test generation algorithms);
    - Design for testability techniques;
    - Verification hierarchy;
    - Simulation-based approach and formal approaches.
- Physical Synthesis (PS):
    - Basic PS concepts and standard cell-based design;
    - Netlist and system partitioning;
    - Chip planning;
    - Global and detailed placement;
    - Global routing;
    - Detailed routing;
    - Specialized routing;
    - Timing Closure.
- EDA practical aspects: prototype implementation of selected technique.

7) Textbooks:

[1] WANG, Laung-Terng ; CHANG, Yao-Wen ; CHENG, Kwang-Ting (Tim). **Electronic Design Automation: Synthesis, Verification, and Test** (Systems on Silicon). Morgan Kaufmann. 1st edition (March 12, 2009) ISBN-10: 0123743648 ISBN-13: 978-0123743640 https://www.sciencedirect.com/science/book/9780123743640

[2] KAHNG, Andrew B.; LIENIG, Jens; MARKOV, Igor L.; HU, Jin. **VLSI Physical Design**: From Graph Partitioning to Timing Closure. Dordrecht: Springer, 2011. 310 p. ISBN-13: 978-9048195909

8) Complementary Bibliography:

[3] CORMEN, Thomas H.; LEISERSON, Charles E.; RIVEST, Ronald L.; STEIN, Clifford. **Introduction to Algorithms.** The MIT Press; 3rd edition (July 31, 2009) ISBN-10: 0262033844 ISBN-13: 978-0262033848.

[4] WESTE, Neil; HARRIS, David. **CMOS VLSI Design:** a circuits and systems perspective. Addison-Wesley, 4th Edition, 2010. ISBN 978-0321547743.

[5] LAVAGNO, Luciano; MARKOV, Igor L.; MARTIN, Grant E.; SCHEFFER, Louis K. **Electronic Design Automation for Integrated Circuits Handbook**, Second Edition - (Two Volume Set). CRC Press; 2 edition (May 5, 2016) ISBN-10: 1482254506 ISBN-13: 978-1482254501

[6] De Micheli, Giovanni. **Synthesis and Optimization of Digital Circuits.** McGraw-Hill, 1994) ISBN-10: 0070163332 ISBN-13: 978-0070163331.

[7] MARTIN, Grant. **ESL Design and Verification:** a prescription for electronic system level methodology (Systems on Silicon) Morgan Kaufmann, 2007. 1st Edition. ISBN-10: 0123735513 ISBN-13: 978-0123735515

[8] WILE, Bruce, GOSS, John; ROESNER, Wolfgang. **Comprehensive Functional Verification**. Morgan Kaufmann, 2005.

[9] ALPERT, Charles J.; MEHTA, Dinesh P.; SAPATNEKAR, Sachin S. (Editors) **Handbook of Algorithms for Physical Design Automation.** [S.l.]: Auerbach Publications, 2008. 1024 p. ISBN-13: 978-0849372421

[10] LIM, Sung Kyu. **Practical Problems in VLSI Physical Design Automation.** Dordrecht: Springer; 2008. 264 p. ISBN-13: 978-1402066269

[11] Selected papers of state-of-the-art EDA techniques.